



# **PCI Express 2.0 Serial Data Operator's Manual**

**Revision A – February, 2008**

**Relating to the Following Release Versions:**

- **Software Version Rev. 5.3.0.X**

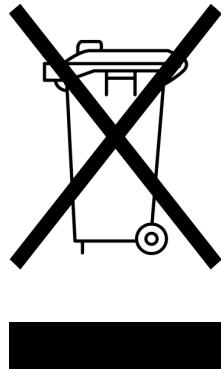
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## INTRODUCTION TO PCI EXPRESS 2.0

PCI Express was developed by Intel as a computer interface to replace PCI (Peripheral Component Interconnect), PCI-X, and AGP (Advanced Graphics Port). It was introduced in 2004 and the specifications are now being further developed by the PCI Special Interest Group, or **PCI SIG**.

### Some History

Unlike PCI, a parallel bus, PCI Express has serial point to point dual simplex links. Each link is made up of 1, 4, 8, 16 or 32 lanes, 1 lane and 16 lane connectors are common today. A by-1 (1 lane) PCIe connector is very small, a by-16 PCIe connector is approximately the same size as a PCI connector. One lane of PCIe at the original speed of 2.5Gb/s transfers data somewhat faster than a typical PCI slot. 16 lanes transfer data 16 times faster, which is faster than any PCI slot or AGP slot.

PCIe is an example of a trend away from parallel buses to fast serial connections. Other examples include Serial ATA and SAS (Serial Attached SCSI).

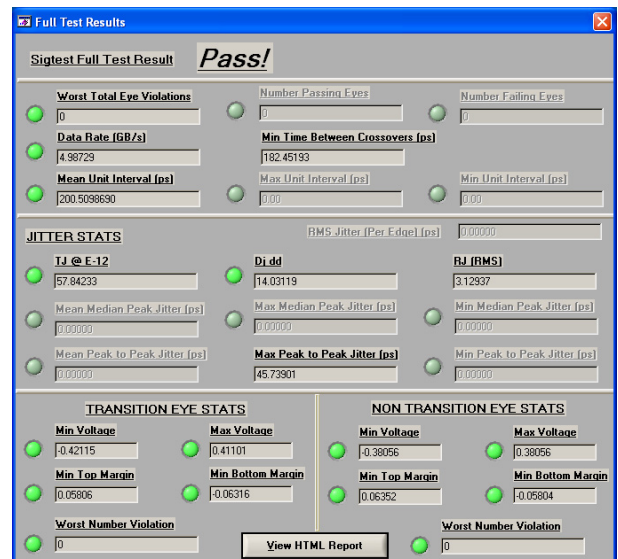
### Revisions and Specifications

After PCIe was introduced, it was revised and became PCIe 1.1, an improved 2.5GT/s (gigatransfer per second) specification. Most PCIe cards are now PCIe 1.1 cards. PCIe revision 2.0 specifications were released in December 2006. PCIe 2.0 covers both 2.5GT/s and 5GT/s. 5GT/s doubles the original data transfer rate per lane. To allow 5GT/s over the same paths and through the same connectors as used for 2.5GT/s, a new 6dB de-emphasis setting was permitted at 5GT/s. The PCI-SIG will commence official testing of PCIe 2.0 cards and systems in September 2008.

PCIe revision 3 specifications are being developed. The PCI-SIG has already announced a data rate of 8GT/s. However, the data will no longer be 8B/10B coded, which was a 25% overhead, so revision 3 will double the data transfer of 5GT/s revision 2.

For each revision, there are two PCIe specifications. Both are important for designers of system boards and add-in cards. They are the PCI Express Base Specification (the “Base spec”) and the PCI Express Card Electromechanical Specification (the “CEM spec”).

- **The Base spec** specifically addresses designing a board. The Base spec revision 2.0 introduces several measurements and several filters unique to PCIe; it mandates that transmitted signal measurements be made at the transmitting chip’s pins or that the effects of any fixture be removed; and for some measurements it mandates at least 12.5GHz bandwidth.
- **The CEM spec** addresses testing completed system boards or add-in cards. For electrical testing, it uses official fixtures supplied by the PCI-SIG taking the effect of these fixtures into account in the limits it requires to be met. Transmitted signal testing involves capturing one million consecutive UI of data (and the clock simultaneously, for system boards) and then giving the waveforms to the official compliance test software, SIGTEST, available from the PCI-SIG’s website. Both parametric and eye diagram mask tests are required by the CEM spec. This testing is done at workshops. The goal of the CEM spec is to make relevant, simple tests that can be completed in the limited time of available in a workshop setting.



## CARD ELECTRO-MECHANICAL (CEM) TESTING

Although, official CEM testing is done by acquiring the appropriate waveforms and running SIGTEST, the SDA can approximate these measurements. The following steps show how the SDA can be used to approximate CEM testing.

**Note:** See LeCroy's PCI Express 2.0 Website for more information about official CEM testing include our Test Methodology.  
[www.lecroy.com/tm/Options/Software/PCIExpressGen2](http://www.lecroy.com/tm/Options/Software/PCIExpressGen2)

1. Click the **Analysis** → **Serial Data**.

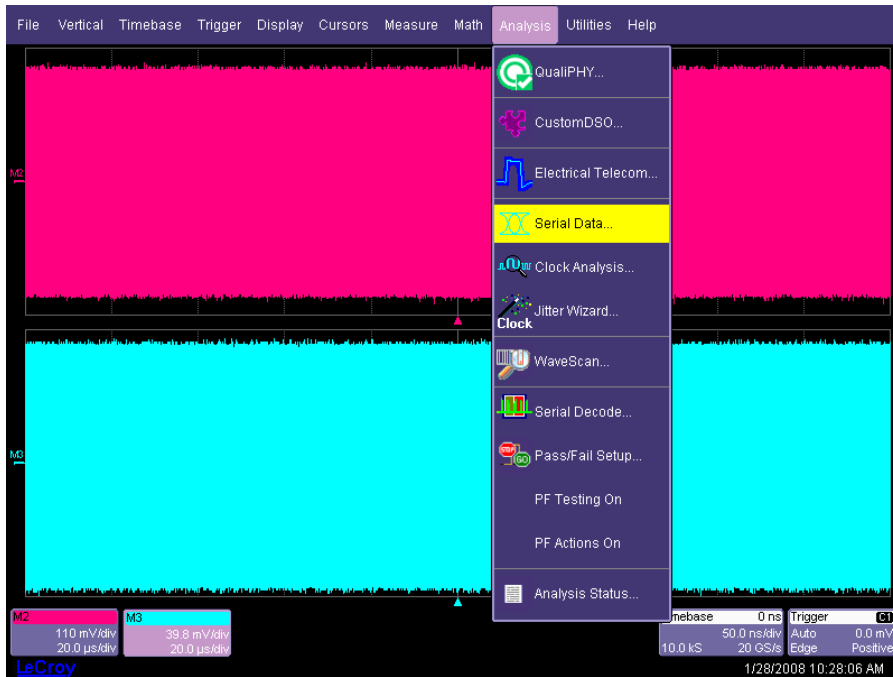
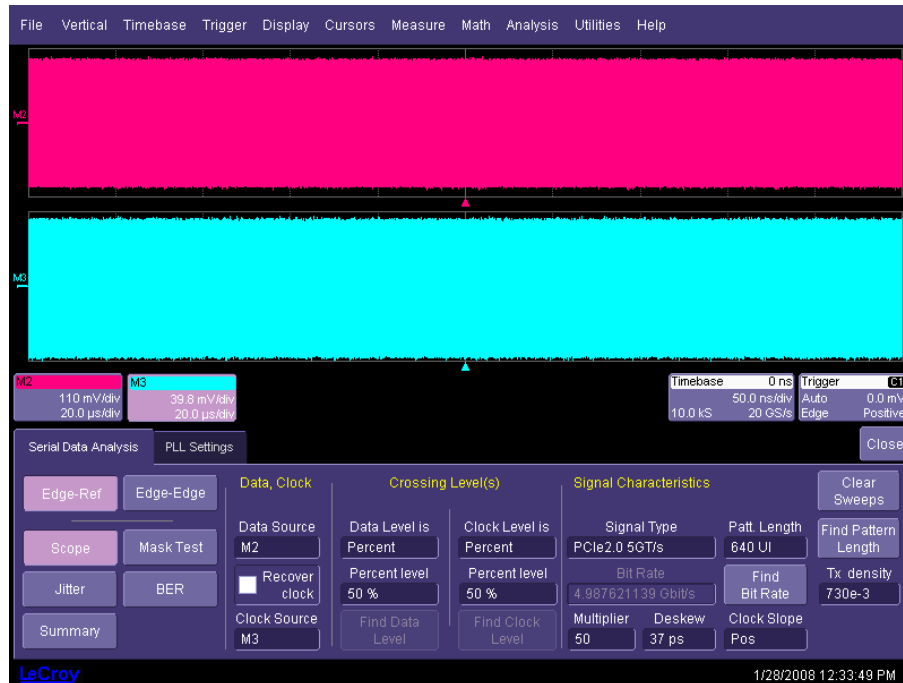


Figure 1. Analysis menu

- The **Serial Data Dashboard** is then shown. Set up all of the necessary parameters to perform measurements on several Serial Data standards including PCI-Express 2.0 from the following screen.



**Figure 2. Serial Data Analysis dashboard**

Define the following parameters:

- **Signal Type.** For PCI-Express 2.0 Testing the appropriate **Signal Type** is PCIe2.0 5GT/s.
- **Data Source.** Select what channel or memory location the data is coming from.

**Note:** For PCI-Express 2.0 testing it is acceptable to use a recovered clock for Add-in card testing. However, for System testing, the actual clock signal must be analyzed. As per the PCI-Express Specification, the Data and the Clock signal must be captured simultaneously.

- For system board testing, un-check the **Recover Clock** checkbox and specify the clock source. When using a clock signal, the user must specify how many times the clock frequency must be multiplied to get the data frequency. For PCI-Express 2.0 this **Multiplier** must be set to **50** and the **Clock Slope** must be set to **Pos**. At this point, an appropriate PLL must be selected.

3. Click the **PLL Settings** tab and choose any of the 3 PCI-Express 2.0 PLLs.

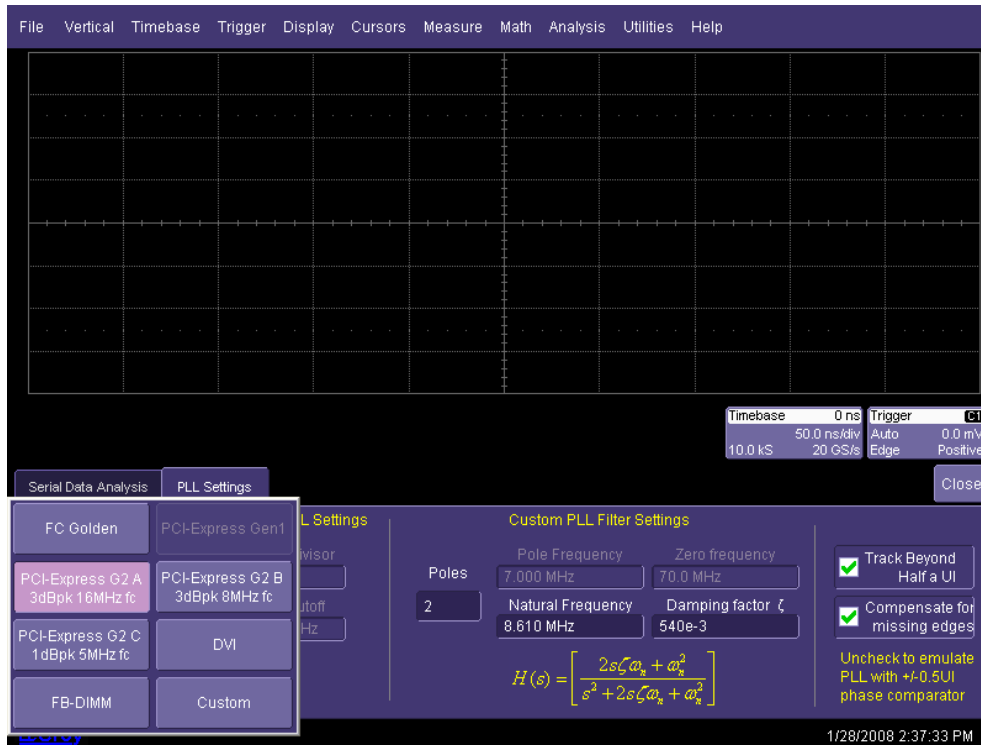


Figure 3. PLL Settings menu

The 3 PCI-Express 2.0 PLLs are:

- **PCI-Express G2 A 3dBpk 16MHz fc**
- **PCI-Express G2 B 3dBpk 8MHz fc**
- **PCI-Express G2 C 1dBpk 5MHz fc**

**Note:** For compliance testing, the user must run the test with all 3 PLLs and take the worst case results.

4. Once an appropriate PLL is selected the user can return to the **Serial Data Analysis** tab. Now the user can click the **Find Bit Rate** button and the **Find Pattern Length** button to have the SDA automatically detect the Bit Rate and Pattern Length (See Figure 2). To center the eye in the mask, a **Deskew** value can also be entered.

At this point, the user is ready to begin testing. All of the standard Serial Data Analyzer capabilities are available for PCI-Express 2.0 testing.



## MASK TEST

Click the **Mask Test** button in the **Serial Data Analysis** dashboard to test waveforms against any of the fourteen 2.0 masks defined by the PCI-SIG (Table 1). To view the transition and non-transition eyes, select **Transition** from the **Mode** dialog.

Notice how you can choose 2 separate masks to display. For this test we have chosen **System Bd TX trans and non-trans with XTalk**. Since this mask has both the transition and non-transition mask, we can select this for both the **Mask Type** and the **Mask Type (Eye 2)** settings.

See Table 1 for a list of the masks as defined by the PCI-SIG. See Table 2 for a description of what masks should be used for each type of signal.

Mask testing requires that the oscilloscope channels be deskewed in order to properly align the eye with the mask.

**Note:** Reference the **Deskew Procedures** section of this manual for more information.

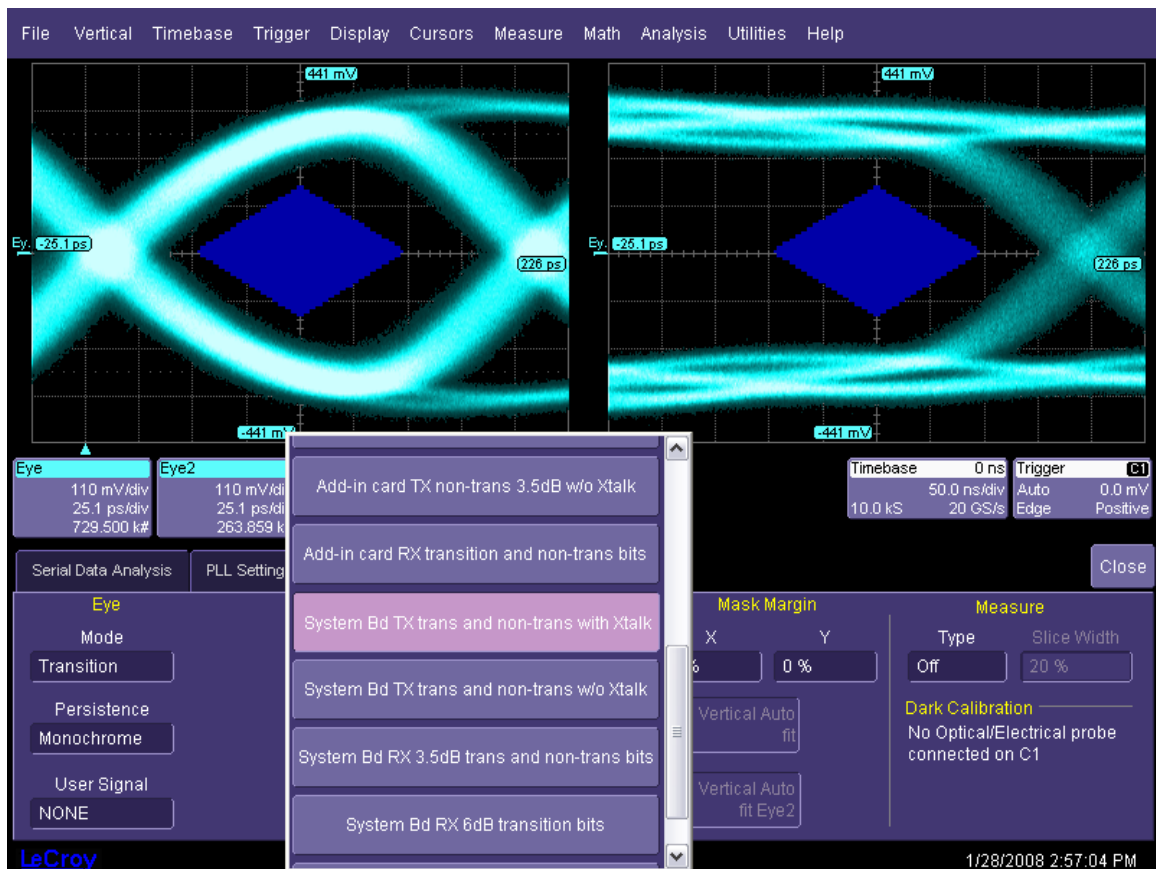


Figure 4. Mask Test menu

Mask	Board	Speed	TX/RX	dB	Transition	XTALK
1. Add-in card TX non-trans 6 dB with XTALK	Add-in	5 GT/s	TX	6	non	with
2. Add-in card TX trans 6 dB with XTALK	Add-in	5 GT/s	TX	6	trans	with
3. Add-in card TX non-trans 6 dB w/o XTALK	Add-in	5 GT/s	TX	6	non	without
4. Add-in card TX trans 6 dB w/o XTALK	Add-in	5 GT/s	TX	6	trans	without
5. Add-in card TX non-trans 3.5 dB with XTALK	Add-in	5 GT/s	TX	3.5	non	with
6. Add-in card TX trans 3.5 dB with XTALK	Add-in	5 GT/s	TX	3.5	trans	with
7. Add-in card TX non-trans 3.5 dB w/o XTALK	Add-in	5 GT/s	TX	3.5	non	without
8. Add-in card TX trans 3.5 dB w/o XTALK	Add-in	5 GT/s	TX	3.5	trans	without
9. Add-in card RX trans and non-trans bits	Add-in	5 GT/s	RX	3.5 and 6	both	---
10. System Bd TX trans and non-trans with XTALK	System	5 GT/s	TX	3.5 and 6	both	with
11. System Bd TX trans and non-trans w/o XTALK	System	5 GT/s	TX	3.5 and 6	both	without
12. System Bd RX 3.5 dB trans and non-trans bits	System	5 GT/s	RX	3.5	both	---
13. System Bd RX 6 dB transition bits	System	5 GT/s	RX	6	trans	---
14. System Bd RX 6 dB non-transition bits	System	5 GT/s	RX	6	non	---

**Table 1. Eye diagram masks**

Add-in or System	Transmit or Receive	Bit Rate	De-Emphasis	Mask (References Table 1)
Add-in	Transmit	5 GT/s	3.5 dB	5 and 6 (with XTALK) or 7 and 8 (without XTALK)
Add-in	Transmit	5 GT/s	6 dB	1 and 2 (with XTALK) or 3 and 4 (without XTALK)
Add-in	Receive	5 GT/s	3.5 dB	9
Add-in	Receive	5 GT/s	6 dB	9
System	Transmit	5 GT/s	3.5 dB	10 (with XTALK) or 11 (without XTALK)
System	Transmit	5 GT/s	6 dB	10 (with XTALK) or 11 (without XTALK)
System	Receive	5 GT/s	3.5 dB	12
System	Receive	5 GT/s	6 dB	13 and 14

**Table 2. Conditions for using each mask**

## JITTER

From the **Serial Data Analysis** tab, the user can also chose the **Jitter** button. All of the jitter testing capability of the Serial Data Analyzer is available from this menu (see following figures).

The **Filtered Jitter Type** dialog has 2 new Jitter Filters as specified by the PCI-SIG (see Figure 6). These filters are:

1. **PCieG2Hhi**
  - Unity gain above 1.5 MHz inclusive
  - 0.001 gain below 1.5 MHz
2. **PCieG2Hlo**
  - Bandpass unity gain from 10 KHz to 1.5 MHz inclusive
  - 0.001 gain elsewhere

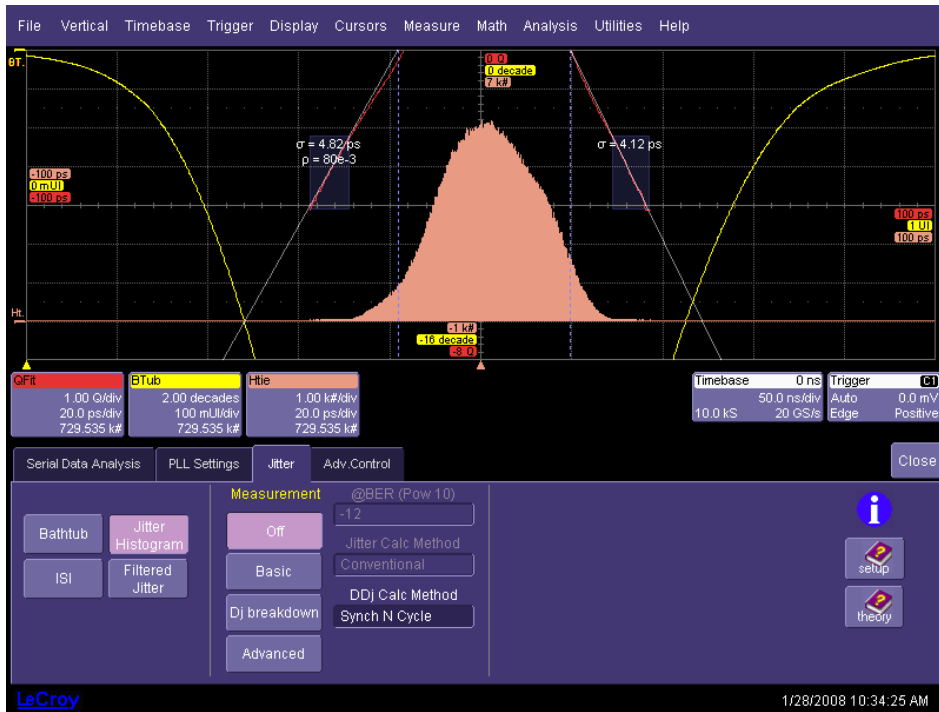


Figure 5. Jitter menu

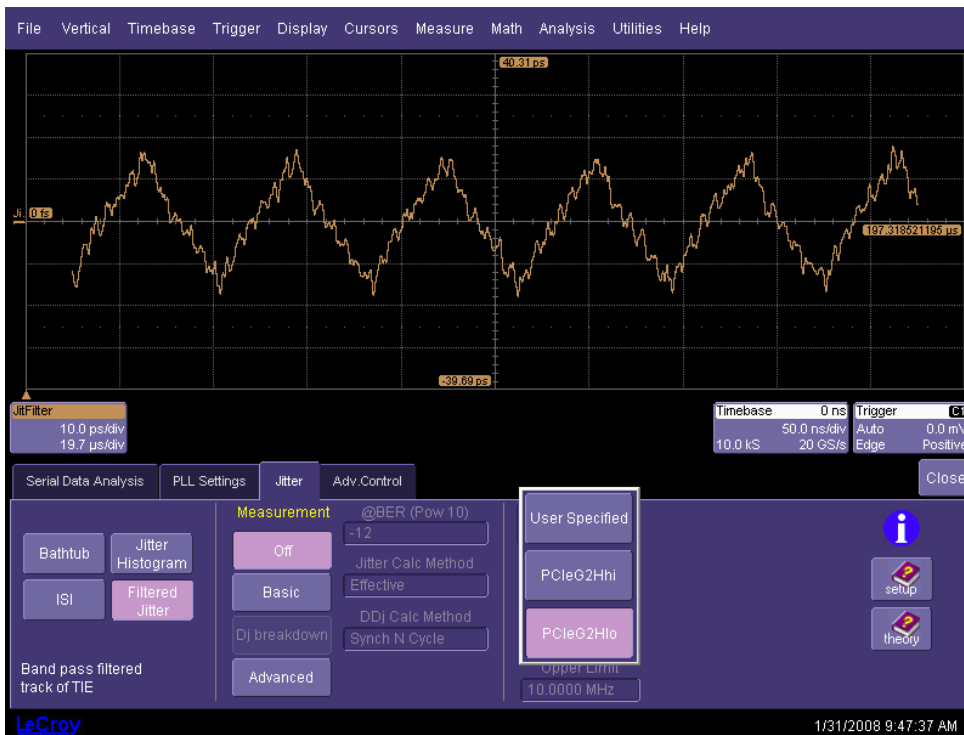


Figure 6. Jitter Filter Types

## BIT ERROR RATE

The standard Bit Error Rate capabilities are available for PCI-Express 2.0. All of the standard SDA capabilities are available from this menu.

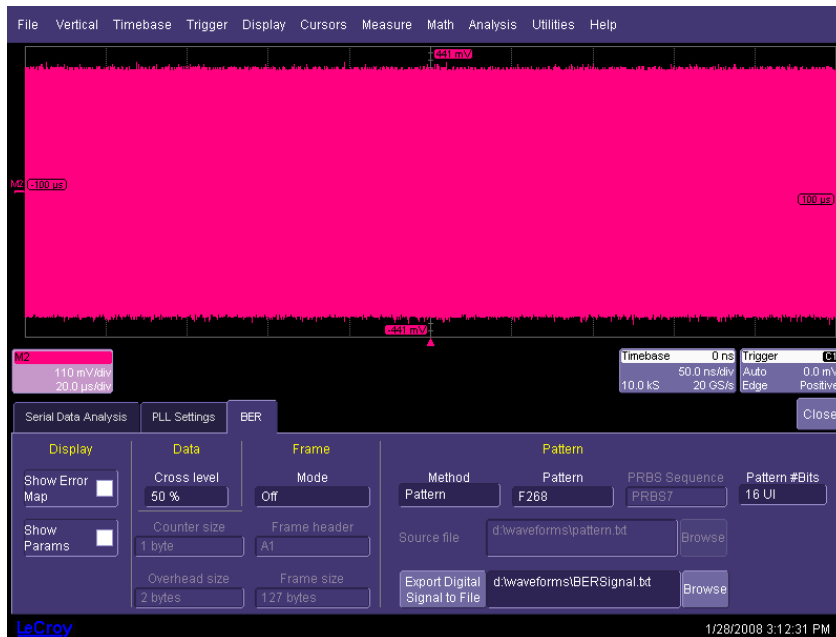


Figure 7. BER menu

## SUMMARY VIEW

The standard Summary view capabilities are available for PCI-Express 2.0.

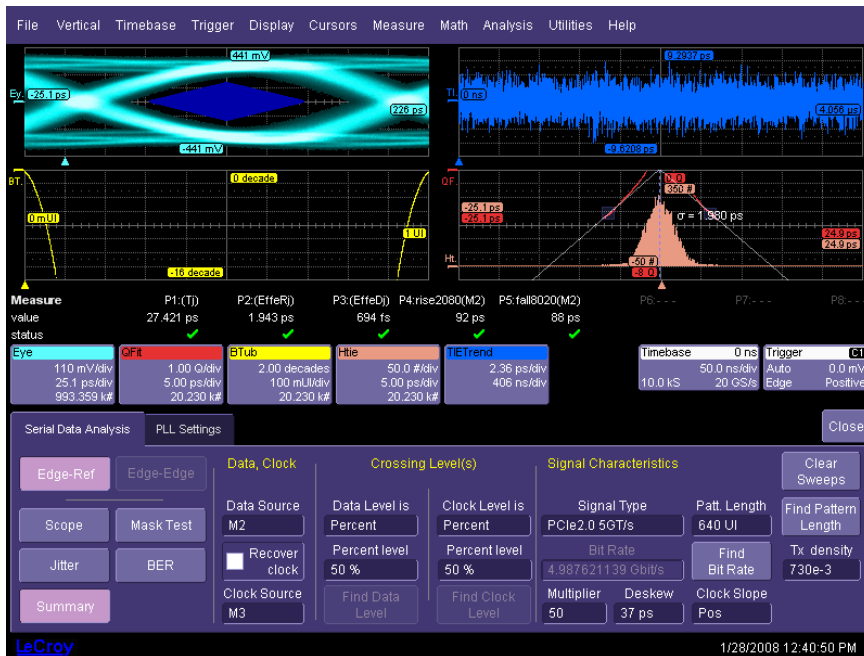


Figure 8. Summary view

## TESTING USING SIGTEST

For information on how to use a LeCroy Serial Data Analyzer with SigTest please see the LeCroy Test Methodology that is available on the LeCroy website and the PCI-SIG website, respectively:

- <http://www.lecroy.com/tm/Options/Software/PCIExpressGen2/>
- [http://www.pcisig.com/specifications/pciexpress/compliance/compliance\\_library](http://www.pcisig.com/specifications/pciexpress/compliance/compliance_library)

## BASE SPEC TESTING

See PCI Express Base Specification rev. 2.0 Table 4.13.

Item	What we do	Additional Information
<b>UI</b>	BitRate parameter	BitRate produces a value in bits per second. Use parameter math, invert to get period as table 4.13 shows. Or, since +/-300ppm from 5Gb/s is +/- 1.5Mb/s, we can compare the bit rate result to 4.9985 Gb/s min 5.0015Gb/s max.
<b>VTxDiffP-P</b>	VTxDiffP-P	New parameter.
<b>VTxDiffP-PLow</b>	VTxDiffP-P	Same measurement as VTxDiffP-P, just a different signal case.
<b>Vtx-de-ratio-3.5dB</b>	VTxDeRatio	Parameter.
<b>Vtx-de-ratio-6dB</b>	VTxDeRatio	Parameter.
<b>Tmin-pulse</b>	TMinPIs	New parameter. For base spec measurement, jitter caused by de-emphasis should be removed. This is done using Eye Dr. (described later in this manual).
<b>Ttx-eye</b>		Requires removing de-emphasis, using Eye Dr. After that we make eye diagrams and measure eye width.
<b>Ttx-hf-dj-dd</b>	Filtered Jitter	Turn on basic jitter parameters. Use Effective jitter decomposition. Set the Jitter Filter to PCIeG2Hhi. Look at DJ. Requires removing de-emphasis, using Eye Dr.
<b>Ttx-lf-rms</b>	Filtered Jitter	Same as previously mentioned except set the Jitter Filter to PCIeG2Hlo. Look at RJ (Alternative: select Advanced jitter, look at RMS).
<b>Ttx-rise-fall</b>	TxRise, TxFall	New parameters (before firmware 5.2 parameters with these names existed, but measurement was not as described in Gen2 Base spec).
<b>Trf-mismatch</b>	TxRise, TxFall	The difference between TxRise and TxFall.
<b>BWtx-pll-...</b>		Procedure - not a single measurement. Requires modulating PCIe clock at different frequencies, measuring jitter.
<b>RLtx-diff</b>	SDA100G TDR	Differential return loss.
<b>RLtx-cm</b>	SDA100G TDR	Common mode return loss.
<b>Ztx-diff-dc</b>		Source impedance during signaling. This parameter is captured for 5.0 GT/s by RLTX-DIFF. Specification is <120 ohms for 5GT/s; 80 to 120 ohms for 2.5GT/s.

Item	What we do	Additional Information
<b>Vtx-cm-ac-p</b>	CMACp	Parameter $RMS[(V_{D+} + V_{D-})/2 - DC_{AVG}(V_{D+} + V_{D-})/2]$ during L0. Defined for 2.5GT/s.  Note: L0 is the normal operating state, where data and control packets can be transmitted and received. Defined in section 4.2.5.5 of the Base Spec.
<b>Vtx-cm-ac-pp</b>		Slightly different 5GT/s measurement: $\max(V_{D+} + V_{D-})/2 - \min(V_{D+} + V_{D-})/2$
<b>ltx-short</b>		short circuit current limit.
<b>Vtx-dc-cm</b>	mean	Parameter. Limits are 0V to 3.6V.
<b>Vtx-cm-dc-active-idle-delta</b>	mean	Difference in mean in L0 and in electrical idle.
<b>Vtx-cm-dc-line-delta</b>	mean	Vtx-cm-dc on D <sup>+</sup> minus Vtx-cm-dc on D <sup>-</sup> during L0.
<b>Vtx-idle-diff-ac-p</b>	filter, pkpk	Electrical idle peak differential voltage AC. Subtract D <sup>+</sup> - D <sup>-</sup> , high pass filter according to the spec (to filter inside the oscilloscope requires DFP option), use pkpk parameter on that
<b>Vtx-idle-diff-dc</b>	filter, pkpk	Electrical idle peak differential voltage DC. Subtract D <sup>+</sup> - D <sup>-</sup> , low pass filter according to the spec (requires DFP), use pkpk parameter on that.
<b>Vtx-rcv-detect</b>	(cursors)	Receive detect: the transmitter swings voltage positive, up to 600mV max. Trigger on that, capture it, and measure the max voltage.
<b>Ttx-idle-min</b>		Minimum time required to be spent in electrical idle. This measurement should be made by a protocol analyzer - that will read time of these events directly.
<b>Ttx-idle-set-to-idle</b>		Time between electrical idle ordered sets and the TX meeting all electrical idle specs. A protocol analyzer would provide a convenient way to trigger the oscilloscope on the EIOS. Capture differential data, and find the time (using measure gate) at which Vtx-cm-dc-line-delta, Vtx-idle-diff-ac-p and Vtx-idle-diff-dc meet specification limits.
<b>Ttx-idle-diff-data</b>		Time from leaving electrical idle to valid differential data signals. The oscilloscope can trigger on the data signal start, assuming it's armed while the TX is in electrical idle.
<b>Tcrosslink</b>		A timeout limit.
<b>Ltx-skew</b>	SD2skew	Skew between two serial data signals. User specifies the pattern to correlate, and the bit rate.
<b>Ctx</b>		Blocking capacitor value.

## UI

Use the bit-rate parameter of the waveform as P1. +/- 300ppm from 5Gb/s is 4.99985 to 5.0015Gb/s. To see the result in ps, set P2 to show the P-Invert math operator on P1.

Look at the result of P2. Note: the +/- 300ppm limit does not account for SSC.

Measure	P1:bitrate(F1)	P2:1/(P1)
value	4.9874 Gbit/s	200.506 ps/bit
status	✓	✓

Details: BitRate is a two pass computation. The first pass finds a fairly coarse estimate of the bit rate. The second pass uses that estimate to compute the number of UI between each pair of rising edges. The result is: time of the last rising edge minus time of the first rising edge, divided by the number of UI in between.

BitRate needs a moderately long record to function optimally. On a suitable waveform where bit rate should work, the possible error (not counting the oscilloscope's timebase) is  $2 * \text{peak jitter} / \text{time between first and last rising edges}$ . This means for 200ps nominal UI, assuming 15% of a UI peak jitter, the possible error is approximately 60ps / acquisition duration. At 5us/div (50us acquisition) the max error from the computation will be <1.2ppm. At 10us/div and above the max error from the computation will be less than 1ppm.

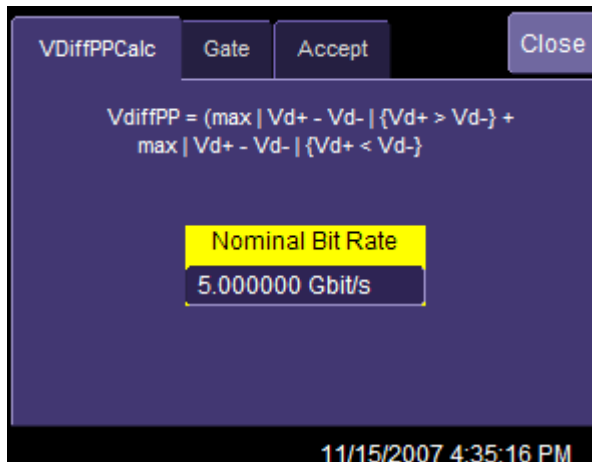
## VTxDiffP-P

This parameter should be used for both the Vdiff cases for 3.5 dB and 6 dB pre-emphasis.

For each UI following a transition, the VDiffPP parameter measures the absolute difference between the max/min voltage in the UI and the min/max voltage in the previous UI that followed a transition.

Measure	P1:VDiffPP(F1)
value	624 mV
status	✓

Requires the user to set the nominal bit rate.



VDiffPPCalc Gate Accept Close

$$VdiffPP = (\max | Vd+ - Vd- | \{Vd+ > Vd-\} + \max | Vd+ - Vd- | \{Vd+ < Vd-\})$$

Nominal Bit Rate

5.000000 Gbit/s

11/15/2007 4:35:16 PM



## VTxDiffP-PLow

Used only in non-de-emphasized case, but uses same exact measurement as VTxDiffP-P.

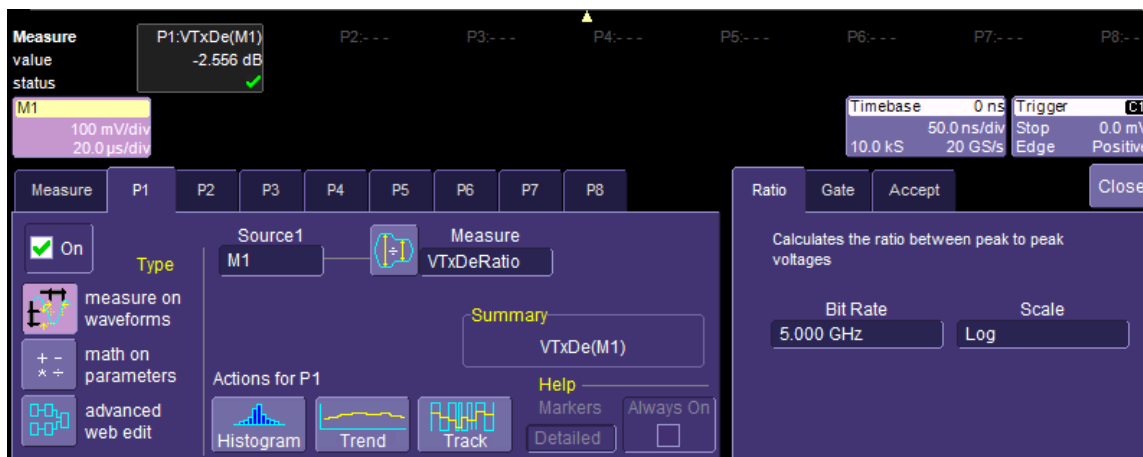
## Vtx-de-ratio-3.5dB

De-emphasis is measured using the VTxDeRatio parameter.

Vtx-de-ratio-3.5dB is this measurement on transmitters with 3.5 dB nominal de-emphasis.

The parameter's setup menu is shown below. You must select the nominal bit-rate and linear or log result scaling. Log scaling produces dB.

The result is computed according to the formula in section 4.3.3.9 of the PCIe Gen2 base specification. The result should be a negative value. Since most of the de-emphasis is used up over several inches of FR4 and the mated PCIe connectors, the result must be made at the TX pins or the effect of the fixture must be removed (which can be done using the Eye Dr Virtual Probing option).



## Vtx-de-ratio-6dB

Measured on transmitters with 6 dB nominal de-emphasis.

Exact same measurement as Vtx-de-ratio-3.5dB, but for a different signal case.

## Tmin-pulse

Tmin-pulse is measured using our TMnPIs parameter.

Minimum time between 50% point of the transitions on each side of a one UI wide pulse. Note that the 50% point can be different on each side of the UI. This is specified in section 4.3.3.8 of the PCIe Gen2 base spec. See figure 4-29 in the base spec.

The setup menu for the TMnPIs parameter is shown below. You must enter nominal bit rate.



## Ttx-eye

Requires removing de-emphasis, using Eye Dr Equalizer Emulation option. The procedure for doing that is documented in an appendix of this manual. The result is used to produce eye diagrams and measure eye width, using normal SDA functionality.

## Ttx-hf-dj-dd

Select **Analysis** → **Serial Data**; then the **Jitter** tab. Turn on basic jitter parameters. Use Effective jitter decomposition in **Jitter Calc Method** dialog. Set the **Jitter Filter Type** to **PCleG2Hhi**. Look at DJ.

## Ttx-lf-rms

Same setup as previously shown, except set the **Jitter Filter Type** to **PCleGen2Hlo**, press **Advanced** and look at rms (in P2).



A word about the jitter filters: The description of the filters in the PCIe base spec demand step changes in the frequency domain response. To get a perfect step in the frequency domain requires an infinitely long FIR filter. If the filtering is done in the frequency domain (as we do it, and as SIGTEST does it), the same requirements apply since multiplication in the frequency domain is the same as circular convolution in the time domain. So, it should be clear that any implementation of these filters on a finite record is an approximation to the perfect step desired in frequency response. In compliance testing, jitter is measured on a 1MS (mega-sample) UI acquisition, for

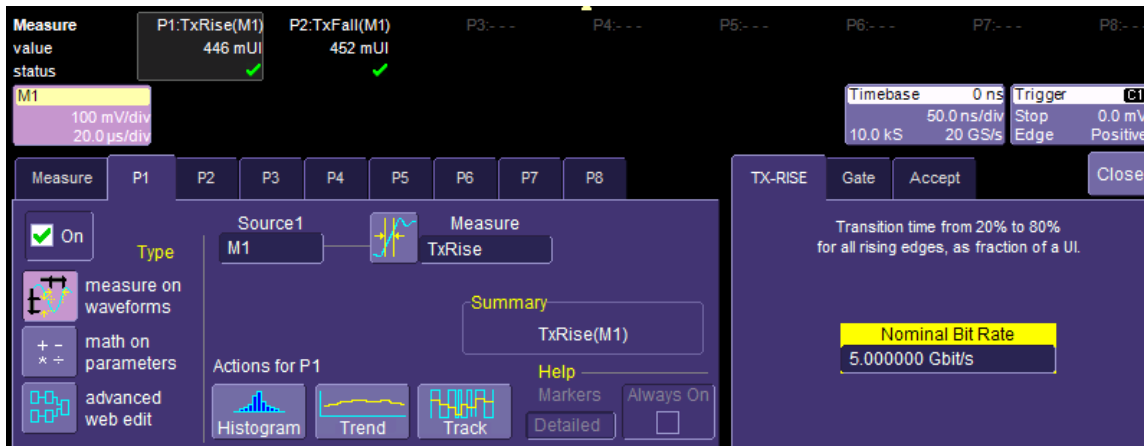
example 8MS at 40GS/s. An 8MS FFT of that has bin spacing of 5KHz. The required filter response is multiplied by the spectrum, and the result is then converted back to the time domain. The beginning and end of the resulting time domain record are significantly disturbed; thinking about the operation as circular convolution we can see why: the long filter shape picked up some data from before the beginning or beyond the end of the waveform in those areas. Since the filter shape should be infinitely long, the entire result is slightly contaminated. However, this effect becomes negligible fairly quickly. We were told that SIGTEST drops the first and last 5% of the result, so we do exactly that also.

## Ttx-rise-fall

This is measured using our TxRise and TxFall parameters. Results are computed according to section 4.3.3.8 of the PCIe Gen2 base spec. See figure 4-29 in the base spec. Transition times are measured from 20% to 80% of each transition. The results are shown in UI.

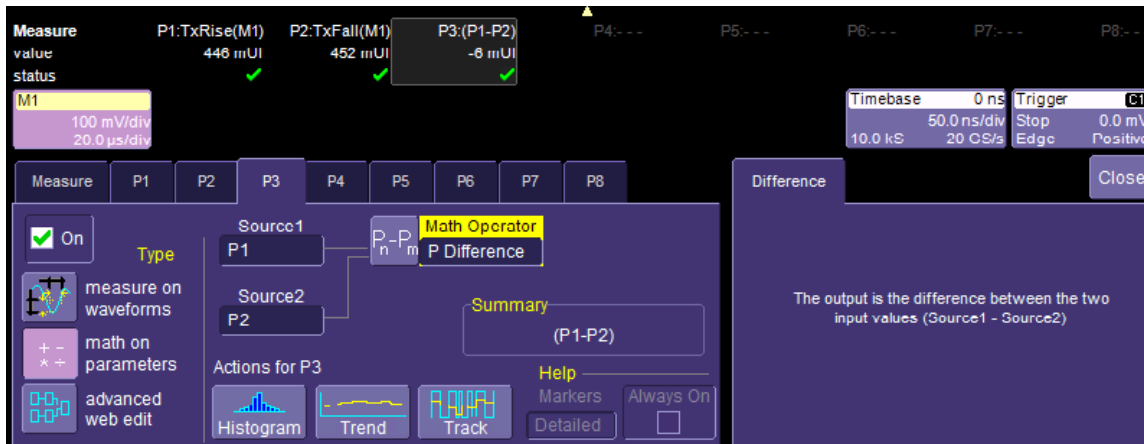
The user must enter the nominal bit rate.

In SDA mask testing, when you select Transition eye diagrams, TxRise and TxFall for transition and non-transition eyes are shown separately beneath each eye diagram, and they are shown in units of seconds. The user doesn't have to enter the nominal bit rate since the SDA code already knows it.



## Trf-mismatch

This is the difference between TxRise and TxFall. At 5.0GT/s, must not exceed 0.1UI. There is no special parameter to calculate this, however it can be produced and shown on the screen simply by setting up one of the parameters to be the difference between TxRise and TxFall, as follows. In the figure below, the difference shown is -6mUI, that is -0.006UI.





## BWtx-pll- and PKG

The PLL bandwidth measurements require equipment besides the oscilloscope, and it requires modulation and measurements at multiple frequencies. In general, some signal must be supplied to phase modulate or frequency modulate the PCIe reference clock. The transmitted data should follow the ref clock modulation at low frequencies, but not at higher frequencies. The modulation on the clock must be measured, and the modulation on the data must be measured at each of multiple modulation frequencies. The result is a Jitter Transfer curve. The PLL bandwidth can be derived from the Jitter Transfer curve by the subtraction  $PLL \text{ response} = 1 - \text{Jitter Transfer}$ . To capture magnitude and phase, the subtraction should be complex, however doing a magnitude only subtraction should be sufficient for sinusoidal modulation.

## RLtx-diff

This measurement needs to be made using either TDR with a sampling oscilloscope such as the LeCroy SDA100G, or a network analyzer.

## RLtx-cm

This measurement needs to be made using either TDR with a sampling oscilloscope such as the LeCroy SDA100G, or a network analyzer.

## Ztx-diff-dc

This is a specification, not a measurement. The PCI Express Base Specification rev 2.0 says "Parameter is captured for 5.0 GHz by  $RL_{TX-DIFF}$ "

## Vtx-cm-ac-p

This is measured using our CMAcP parameter. This requires as input the  $D^+$  and  $D^-$  signals, separately.

Specified for 2.5GT/s, must be  $< 20\text{mV}$ . It is specified as:

$$V_{TX-AC-CM-P} = \text{RMS}[(V_{D^+} + V_{D^-})/2 - DC_{AVG}(V_{D^+} + V_{D^-})/2]$$

Where DC is defined as frequency components below 30KHz.

## Vtx-cm-ac-pp

Specified for 5GT/s, must be  $< 100\text{mV p-p}$ . It is specified as:

$$V_{TX-AC-CM-PP} = \max(V_{D^+} + V_{D^-})/2 - \min(V_{D^+} + V_{D^-})/2$$

This is computed by our peak to peak (pkpk) parameter on the result of a math function that computes the sum of  $D^+$  and  $D^-$  inputs. Therefore the  $D^+$  and  $D^-$  inputs must be supplied as separate inputs.

It is critically important to deskew the cables before making this measurement, since if the  $D^+$  and  $D^-$  edges are not simultaneous that causes common mode spikes.

## Itx-short

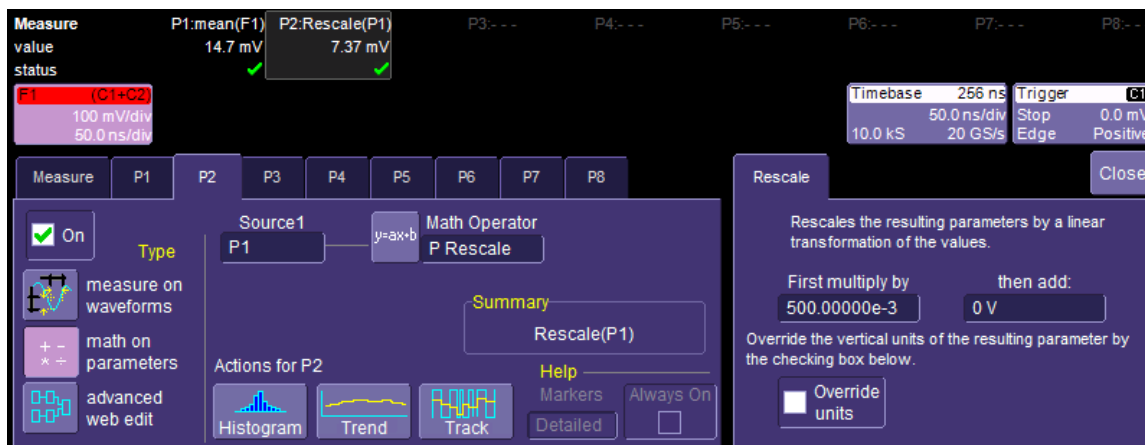
Since the TX is only required to meet this spec when functional differential signals are not being transmitted, this measurement can be made with a current probe that includes a Hall effect sensor, such as the LeCroy CP030. The current probe measures the current flowing through a wire that the head of the current probe surrounds. The

CP030 current probe is the best solution because it allows a true short to be used, and it measures DC current with 1% accuracy. Alternatively, a voltage measurement can be made across a small resistor, the value should be as small as possible since any resistance is not a true short. If one side of the resistor is well grounded then only the voltage on the other side needs to be measured. For example, 90mA across 1 ohm will produce 90mV.

Use the “mean” parameter to compute the average voltage from a reasonably long acquisition (i.e., 50us total or 5us/div).

## Vtx-dc-cm

This is a specification: it is “The allowed DC common-mode voltage at the Transmitter pins under any conditions”. It must be between 0V and 3.6V. This can be measured using the “mean” parameter on the result of a math function that computes the sum of D<sup>+</sup> and D<sup>-</sup> inputs. That means the D<sup>+</sup> and D<sup>-</sup> inputs must be supplied as separate inputs. The result desired is half of the “mean” value. If you want the oscilloscope to produce the result including the divide by two, use the parameter rescale function “P Rescale” to multiply by 0.5, as shown in the figure below.



Remember that the SDA’s offset accuracy specification is  $\pm(1.5\%$  of full scale  $+1.5\%$  of offset value  $+2$  mV). So, at 100mV/div and 0 offset as in the figure above, the measured offset accuracy is within  $\pm 14$ mV.

## Vtx-cm-dc-active-idle-delta

This is the difference between Vtx-dc-cm measurements made in L0 and in Electrical Idle mode. Absolute value of the change must be less than 100mV.

It is the user’s responsibility to switch the device between modes. Designers of a device probably know how to get it into electrical idle. However, here is a simple way to get into and out of electrical idle: Using a PCIe Gen2 compliant motherboard running Windows XP, make Windows XP go to Standby. That should put PCI Express into electrical idle. Windows XP can be configured to go to standby when the power button is pressed; if that is done it gives a one button solution for entering and exiting electrical idle.

## Vtx-cm-dc-line-delta

This is the difference in DC voltage on D<sup>+</sup> and D<sup>-</sup> specified as:

$$|V_{TX-CM-DC-D+} [\text{during } L0] - V_{TX-CM-DC-D-} [\text{during } L0.]] \leq 25\text{mV}$$

Again, this is measured using the “mean” parameter, this time on D<sup>+</sup> and D<sup>-</sup> inputs separately. A long acquisition (i.e., 50us total or 5us/div; that is 2MS at 40GS/s) must be used for accuracy. The difference between the measurements must be within 25mV.

### Vtx-idle-diff-ac-p

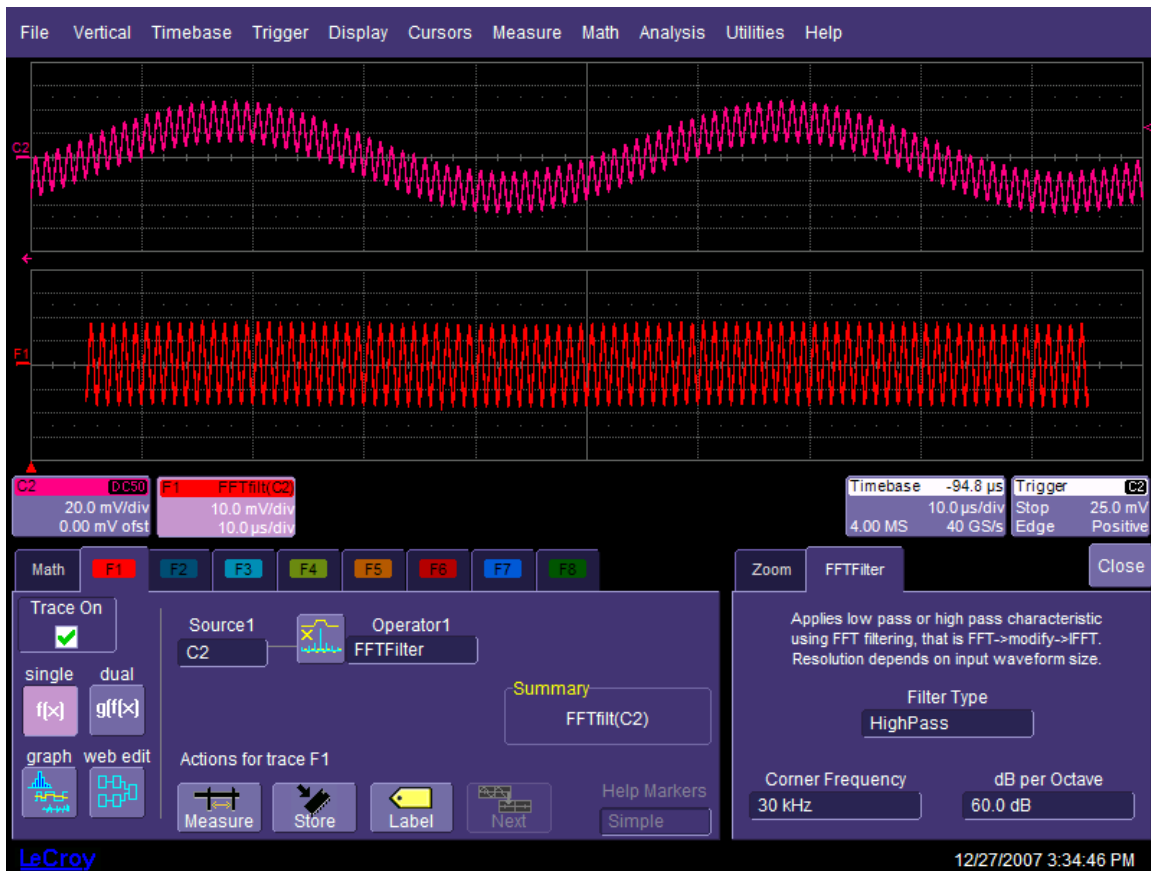
This is a quote from the PCIe Gen2 base spec dated December 20, 2007; table 4-9:

“ $V_{TX-IDLE-DIFFp} = |V_{TX-Idle-D+} - V_{TX-Idle-D-}| \leq 20 \text{ mV}$ . Voltage must be high pass filtered to remove any DC component. Filter characteristics TBD.”

We assume that DC is 30KHz and below, as used elsewhere in the Base specification.

To measure this, either connect  $D^+$  to one channel and  $D^-$  to another channel and use a math function to compute the difference; or use a differential probe such as the LeCroy D13000 connected to one channel. Use (another) math function to apply an FFT Filter to the difference ( $D^+ - D^-$ ). To pass this test, the max of the filtered result should not be greater than 20mV and the min of the filtered result should not be less than -20mV.

In order to see energy down to 30KHz, the time base must be at least 5us/div; please use 10us/div – that gives more resolution in the FFT. Set the filter up as follows – the picture shows 1 MHz sine plus a 20KHz sine being filtered by the FFT filter (The first and last 5% of the result is missing to suppress end effects). The 20kHz sine has been effectively removed from the result:



### Vtx-idle-diff-dc

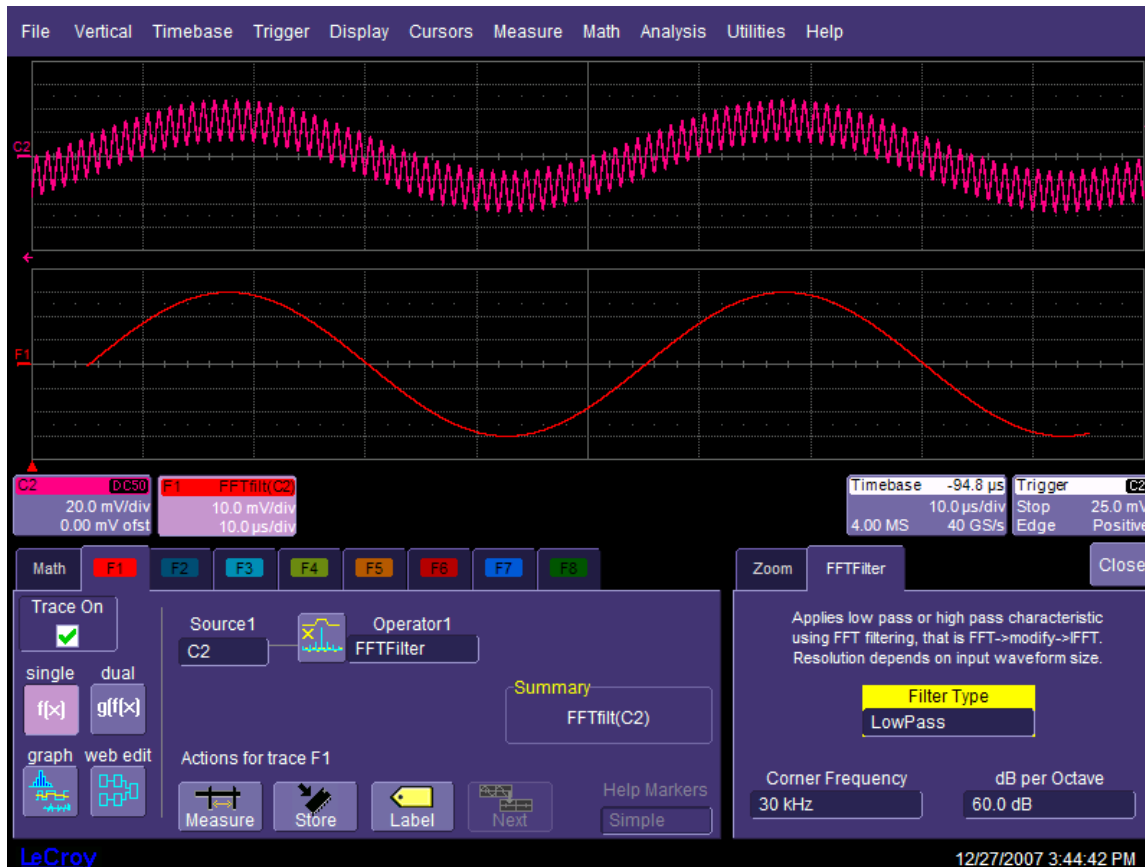
This is a quote from the PCIe Gen2 base spec, table 4-9:

“ $V_{TX-IDLE-DIFF-DC} = |V_{TX-Idle-D+} - V_{TX-Idle-D-}| \leq 5 \text{ mV}$ . Voltage must be low pass filtered to remove any AC component. Filter characteristics complementary to above.”

Where “above” refers to Vtx-idle-diff-ac-p.

Again, we will assume that DC is 30KHz and below, as used elsewhere in the Base specification.

To measure this, set up is the same as for Vtx-idle-diff-ac-p, except the filter is a high pass filter. The filter setup, processing the same example waveform, is shown as follows. Note that this time the 1MHz is removed and the 20kHz remains:



It is the user's responsibility to switch the device between modes. Designers of a device probably know how to get it into electrical idle. However, here is a simple way get into and out of electrical idle: Using a PCIe Gen2 compliant motherboard running Windows XP, make Windows XP go to Standby. That should put PCI Express into electrical idle. Windows XP can be configured to go to standby when the power button is pressed; if that is done it gives a one button solution for entering and exiting electrical idle.

## Vtx-rcv-detect

As the PCIe Gen2 base specification says, this is "The total amount of voltage change in a positive direction that a Transmitter can apply to sense whether a low impedance Receiver is present". The only thing required to make this measurement is to capture D<sup>+</sup> and D<sup>-</sup> while the transmitter is doing receive detection. The voltage can be measured directly on the oscilloscope screen with cursors.

## Ttx-idle-min

Minimum time a Transmitter must be in Electrical Idle (20ns, min).

The oscilloscope can trigger on the absence of data transitions using the "drop out" trigger, to catch transition into electrical idle. It is up to the user to tell the device to exit electrical idle within the minimum time and make sure the transmitter does not come out of electrical idle when told to do so before the minimum time. See section 4.2.6.8.1 of the PCIe Gen2 Base Spec, it says that the receiver "needs to wait a minimum of TTX-IDLE-MIN to start looking for Electrical Idle Exit".

## Ttx-idle-set-to-idle

After sending the required number of EIOSs, the Transmitter must meet all Electrical Idle specifications within this time (8ns max). This is measured from the end of the last UI of the last EIOS to the Transmitter in Electrical Idle.

To measure this, the transmitter must be put into Electrical Idle. The oscilloscope can trigger on the absence of data transitions using the “drop out” trigger, to catch transition into electrical idle. Then, verify that the parameters applying to electrical idle, and to common mode shift from L0 to electrical idle, are all met within 8ns after the last UI of the last EIOS.

## Ttx-idle-diff-data

Maximum time to transition to valid diff signaling after leaving Electrical Idle. (8ns, max).

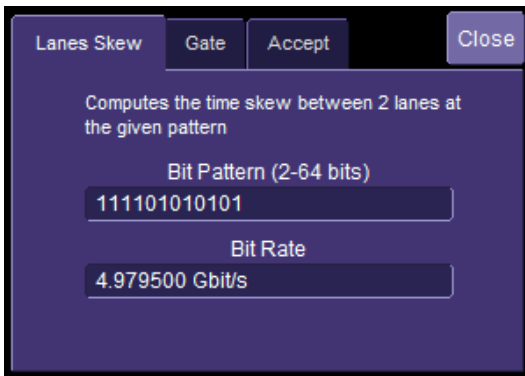
To measure this, after the device is in Electrical Idle, return it to the normal operating state (L0). The oscilloscope can edge trigger on transitions in the data to capture the exit from electrical idle. Verify all the parameters applying to L0 (rise and fall times, DeRatio, common mode, differential amplitude...) are met within 8ns of leaving electrical idle.

## Tcrosslink

This is a spec on the maximum Tcrosslink timeout. This random timeout helps resolve potential conflicts in the crosslink configuration. We think this must be verified in the design. It is probably not practical to measure the “maximum” Tcrosslink timeout.

## Ltx-skew

This measurement is made by our “SD2Skew” (serial data 2 lanes skew) parameter. We recommend doing this on a reasonably short acquisition, 50ns/div works well. An appropriate setup for the compliance pattern and 5GT/s PCIe is shown as follows.



The bit rate should be correct to (at least) four digits. The “BitRate” parameter can be used to get the value to enter in the Bit Rate dialog in this menu. An inaccurate number in the Bit Rate dialog can affect the accuracy of this measurement.

## Ctx

This is a specification on the required size of the AC coupling capacitor. It does not require a measurement made on a signal.



## PLL DESCRIPTIONS

2 poles (and 1 zero) of form:

$$H(s) = \frac{2 \cdot \zeta \cdot \omega_n \cdot s + \omega_n^2}{s^2 + 2 \cdot \zeta \cdot \omega_n \cdot s + \omega_n^2}$$

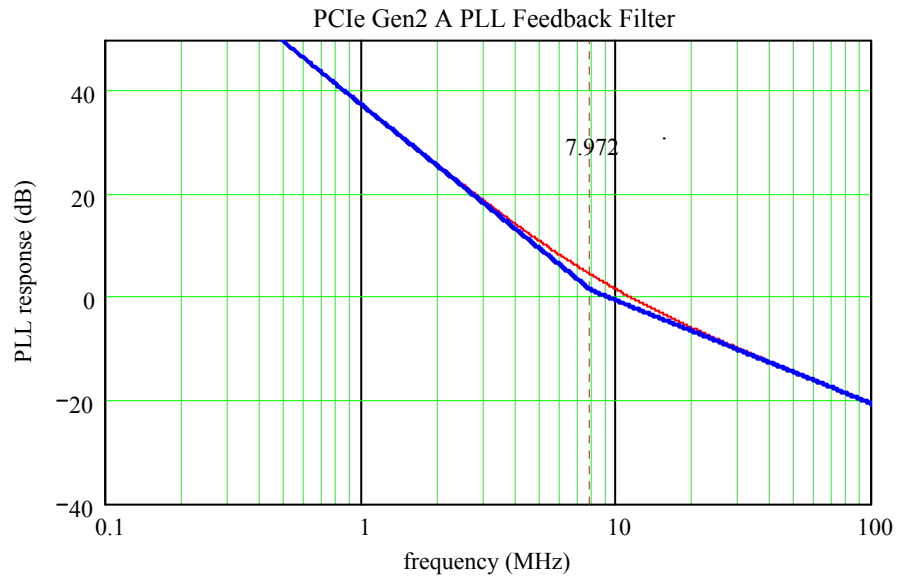
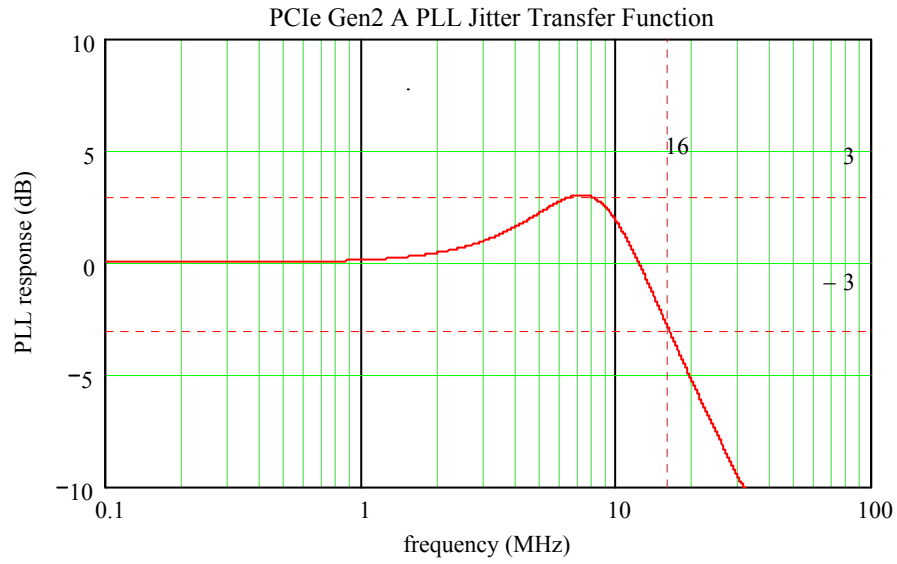
Feedback filter (including integrator and other constants)

$$F(s) = \frac{H(s)}{1 - H(s)} = 2 \cdot \zeta \cdot \omega_n^2 \cdot \frac{s + \frac{\omega_n}{2 \cdot \zeta}}{s^2}$$

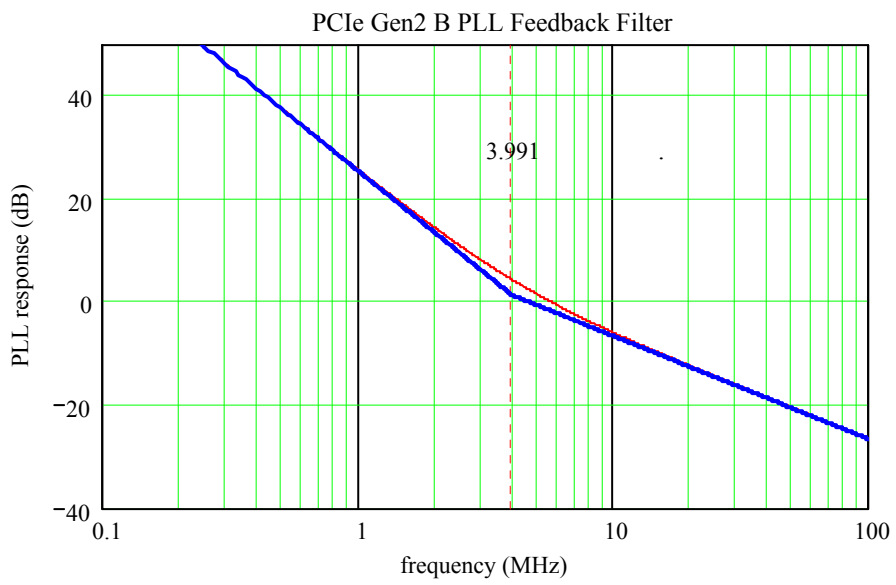
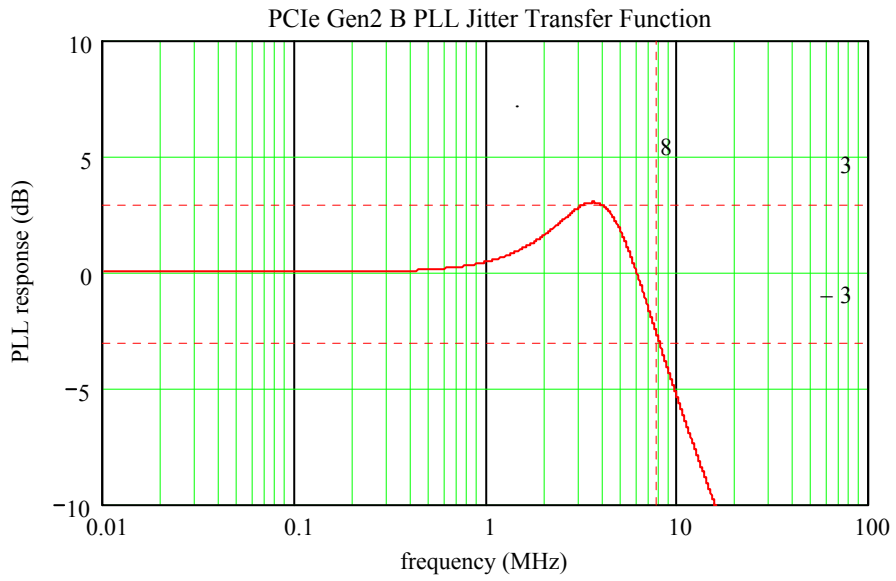
PLL Name	Peak (dB)	Cutoff frequency (-3 dB) (MHz)	Natural frequency (MHz)	zeta
PCI-Express G2 A	3	16	8.610	0.540
PCI-Express G2 B	3	8	4.310	0.540
PCI-Express G2 C	1	5	1.820	1.160

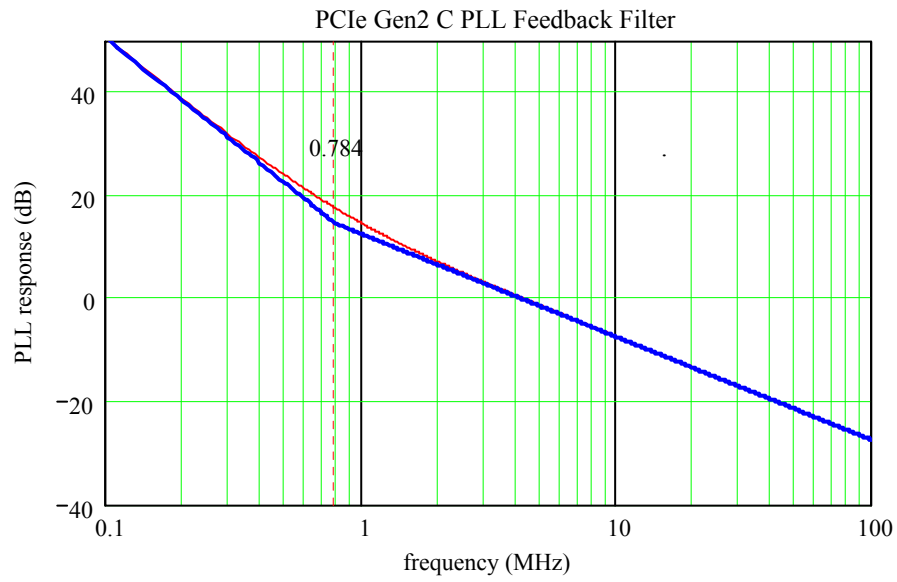
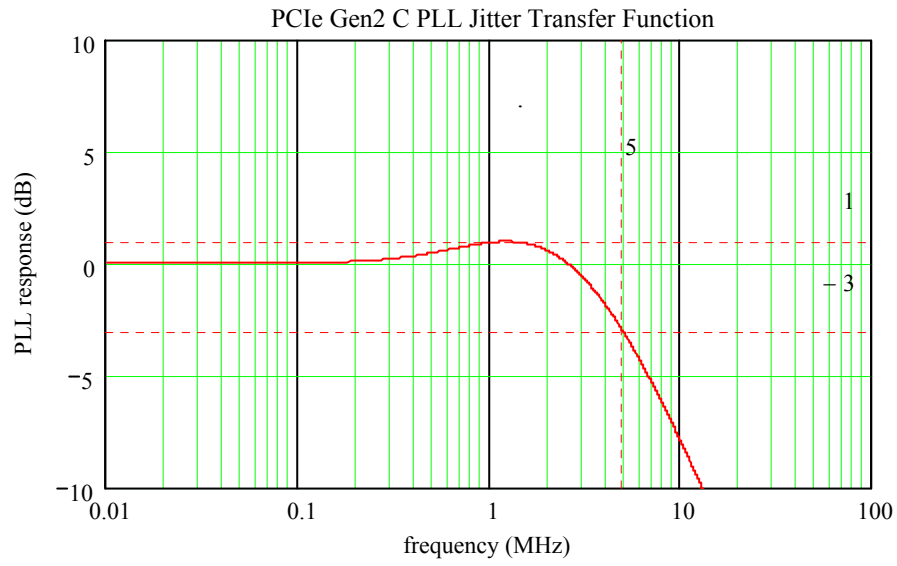
Table 3. PLL descriptions

**PLL A**



PLL B





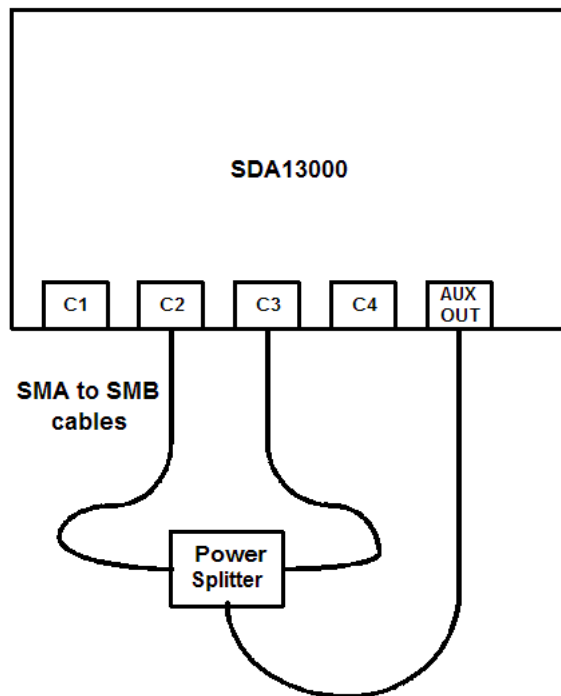
## DESKEW PROCEDURES

Before beginning any test or data acquisition, the oscilloscope must be warmed for at least 20 minutes. Calibration is automatic under software control and no manual calibration is required. The procedure below explains how to compensate for the skew of the cables.

This procedure should be run again if the temperature of the oscilloscope changes by more than a few degrees.

### De-skew using the Aux output

The deskew signal is supplied by the AUX OUT connector on the front panel of the SDA13000. A power splitter is used to supply the same signal to both ends of the cables.



**Figure 9. Configuration for cable skew adjustment**

1. Connect the SMA ends of the cables to be used for probing the data signals to each of the two SMA outputs on the splitter.
2. Connect the input to the splitter to the AUX OUT connector on the SDA13000.
3. Use the **Utilities**→**Utilities Setup...** menu and select the **Aux Output** tab menu to set the AUX OUT signal to a 5 MHz square wave with a 1V amplitude.
4. Display the traces for channel 2 and channel 3. Select **Display**→**Dual Grid** and move the C1 and C2 traces to the same grid using the **Next Grid** button in the channel menus for C2 and C3.
5. Adjust the horizontal scale to 500ps/div.
6. Set the trigger mode to edge with the source as C2.
7. Set the trigger level to 200mV.
8. Define math trace F1 as C1 - C2 and display this trace.
9. Select **Vertical**→**Channel 2 Setup...** and use the **Deskew** dialog in the channel menu to adjust the skew of channel 2 relative to channel 1 so that the 2 traces are lined up on the display.

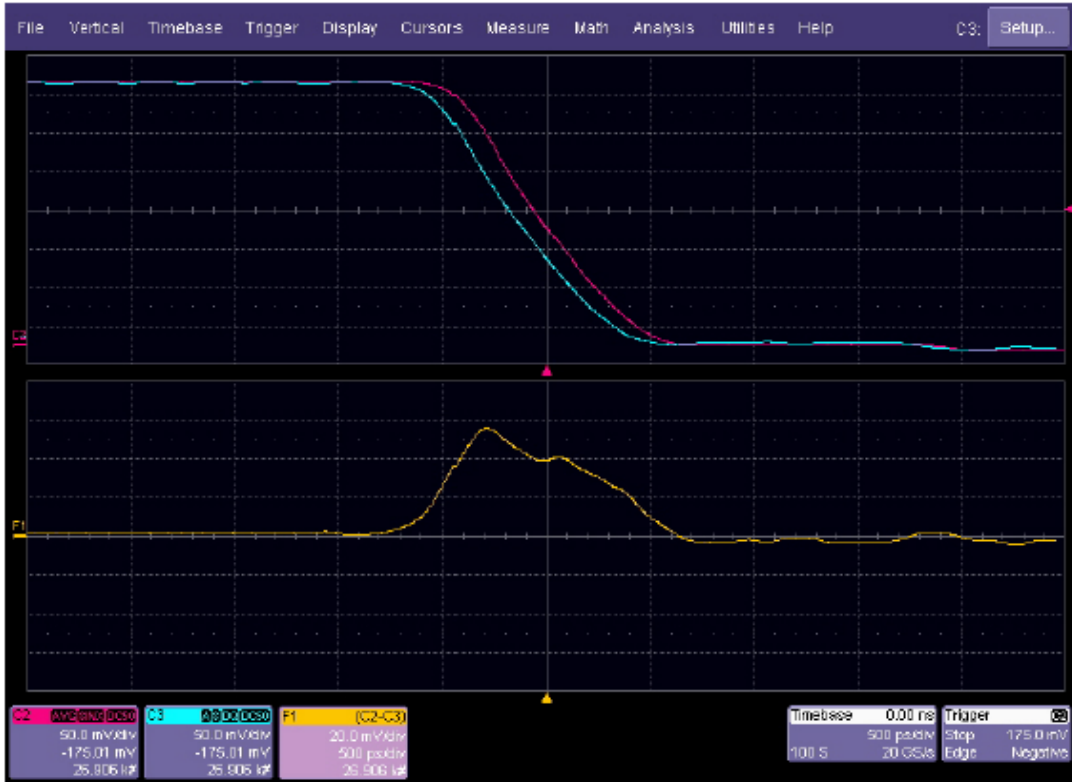


Figure 10. Channels with skew, F1 displays the difference waveform



Figure 11. Channels after skew adjustment, F1 trace appears flat after adjustment

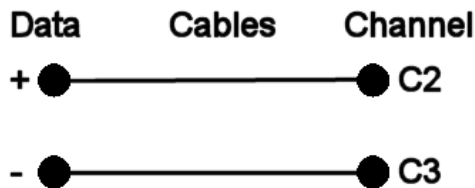
## De-skew using a differential data signal

This is a multi-step procedure which is more complicated than the procedure given above. Its advantages are:

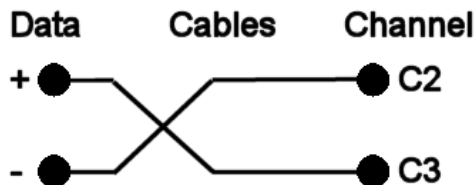
- No adapters needed.
- De-skew at the same V/div settings you'll use to capture your data (because you are capturing your data for this procedure)
- If the differential data signal has higher speed edges than the oscilloscope's AUX OUT, it is easier to get good timing measurements with the faster edges. This is definitely the case for PCI-Express.

Here is the step by step procedure:

1. Connect a differential data signal to C2 and C3 using two approximately matching cables. Set up the oscilloscope as you plan to use it. Set the timebase to capture a few repetitions of the compliance test pattern (at least a few dozen edges). Press **Auto**, so the oscilloscope acquires.



2. On the C3 menu, check **Invert**. Now C2 and C3 should look the same.
3. Using the **Measure Setup**, set P1 to measure the Skew of C2, C3. Turn on **Statistics (Measure menu)**. Write down the mean skew value after it stabilizes. This mean skew value is the addition of Data skew + cable skew + channel skew.
4. Swap the cable connections on the data source side (on the test fixture), and then press the **Clear Sweeps** button on the oscilloscope (to clear the accumulated statistics; since we changed the input).



5. Write down the mean skew value after it stabilizes. This mean skew value is the addition of (-Data skew) + cable skew + channel skew.
6. Add the two mean skew values and divide the sum in half:

$$\frac{[\text{Data skew} + \text{cable skew} + \text{channel skew}] + [(-\text{Data skew}) + \text{cable skew} + \text{channel skew}]}{2}$$

7. The above formula simplifies to:

$$[\text{cable skew} + \text{channel skew}]$$

8. Set the resulting value as the **Deskew** value in C2 menu.
9. Restore the cable connections to their Step 1 settings (previous). Press the **Clear Sweeps** button on the oscilloscope. The mean skew value should be approximately zero - that is the data skew. Typically, results are <1ps given a test fixture meant to minimize skew on the differential pair.
10. On the C3 menu, un-check the **Invert** checkbox and turn off the parameters.

Now the oscilloscope inter-channel skew and cable skew is compensated for, you are ready to test.

The procedure as given above relies on the default setup of the skew parameter (which is: detecting positive edges on both signals, at 50%); C3 was inverted in order to make C2 and C3 both have positive edges at the same time. The default setup of any parameter is in effect at the time it is set up.



§ § §